

CH7516A 4 Lane DisplayPort to 4 Channel LVDS Convertor

FEATURES

General

- Compliant with DisplayPort specification version 1.2 and Embedded DisplayPort (eDP) specification version 1.4
- Support 4 Main Link Lanes at either 1.62Gb/s, 2.7Gb/s, 3.24Gb/s or 5.4Gb/s link rate
- Support VESA and CEA timing standards up to 7680x1080@60Hz or 4800x2160@60Hz with 8/10 bit graphic color depth
- Support Single Port, Dual Ports and Quad ports LVDS output interface
- Crystal Free
- Built in self test mode support
- Hot Plug Detection
- Panel tuning methods support 8-bit+ FRC
- Black panel or Color Bar during invalid input and failure detection
- integrated EDID Buffer up to 2 blocks
- Initiated and controlled by firmware, which is loaded from External BOOT ROM automatically upon power up
- Support BOOT ROM with SPI or I2C interface
- Firmware updated through I2C slave or AUX Channel
- I2C slave support up to 400K Hz
- Programmable power management
- Achieve bit error rate $<10^{-9}$ for raw transport data per lane and symbol error rate $<10^{-12}$ for control data
- Low power consumption
- ESD HBM 4KV
- Offered in a 128-pin QFN package (12.5 x 12.5mm)

DP Receiver

- Compliant with DisplayPort Specification version 1.2 and Embedded DisplayPort (eDP) Specification version 1.2
- Support 4 Main Link Lanes at 1.62Gb/s, 2.7Gb/s, 3.24Gb/s or 5.4Gb/s link rate
- Supports input color depth 6, 8 or 10-bit per pixel in RGB format
- Supports Flexible Lane swap and P/N signal polarity swap on the Main Link Lanes and the AUX channel
- Supports Enhanced Framing Mode
- Support dynamic refresh rate or adaptive sync mode
- Fast and full Link Training for DisplayPort system
- Support eDP Authentication: Alternative Scramble Seed Reset and Alternative Framing
- Support typical 0.5% down spread spectrum clock(SSC) DP input

LVDS Transmitter

- Support Single Port, Dual Ports and Quad ports LVDS

GENERAL DESCRIPTION

Chrontel's CH7516A is a low-cost, low-power semiconductor device that translates the DisplayPort signal to the LVDS in form of RGB. This innovative DisplayPort receiver with integrated 4 channel LVDS transmitters is specially designed to target the AIO and PC market segments. Leveraging the DisplayPort's unique source/sink "Link Training" routine, the CH7516A is capable of instantly bring up the video display to the LCD when the initialization process is completed between CH7516A and the graphic chip.

The CH7516A is designed to meet the DisplayPort specification version 1.2 and the Embedded DisplayPort Specification version 1.4. The 4 Main Link Lanes receiver supports input with data rate running at 1.62Gb/s, 2.7Gb/s, 3.24Gb/s or 5.4Gb/s, and can accept digital RGB signal for LVDS output up to 7680x1080@60Hz or 4800x2160@60Hz.

The CH7516A will convert the DisplayPort signal to LVDS output after DisplayPort Link Training is completed. This feature can be achieved by loading the panel's EDID and the CH7516A's configuration settings in the serial external BOOT ROM connected to the CH7516A. During system power-up and upon completion of the DisplayPort Link Training through AUX Channel, CH7516A will generate LVDS signal according to the panel power-up timing sequencing stored in the external BOOT ROM.

Advanced Region CRC checking and signal failure detection module and the related interrupt mechanism is incorporated in CH7516A, which is specially designed to reduce the risk of signal transmission error in normal consumer or industrial operation.

- output interface with 6/8/10 bit color depth
- Single LVDS port supports up to 140MHz pixel clock frequency
- Support 4 sets TCON Connection with single LVDS port for each set
- Support both OpenLDI (or JEIDA), SPWG (or VESA) and non-JEITA (10-bit only) bit mapping for LVDS application
- LVDS Tx FFE support up to 3 dB Gain
- Flexible LVDS Port Assignment support
- Flexible LVDS output pins swapping
- Spread spectrum control is available for transmitting LVDS signal
- Signal pre-emphasis is programmable for the transmitting LVDS signal, as well as the driver current
- Programmable LVDS Swing and Common Voltage

APPLICATION

- AIO
- Pro-AV system
- PC/IPC motherboard

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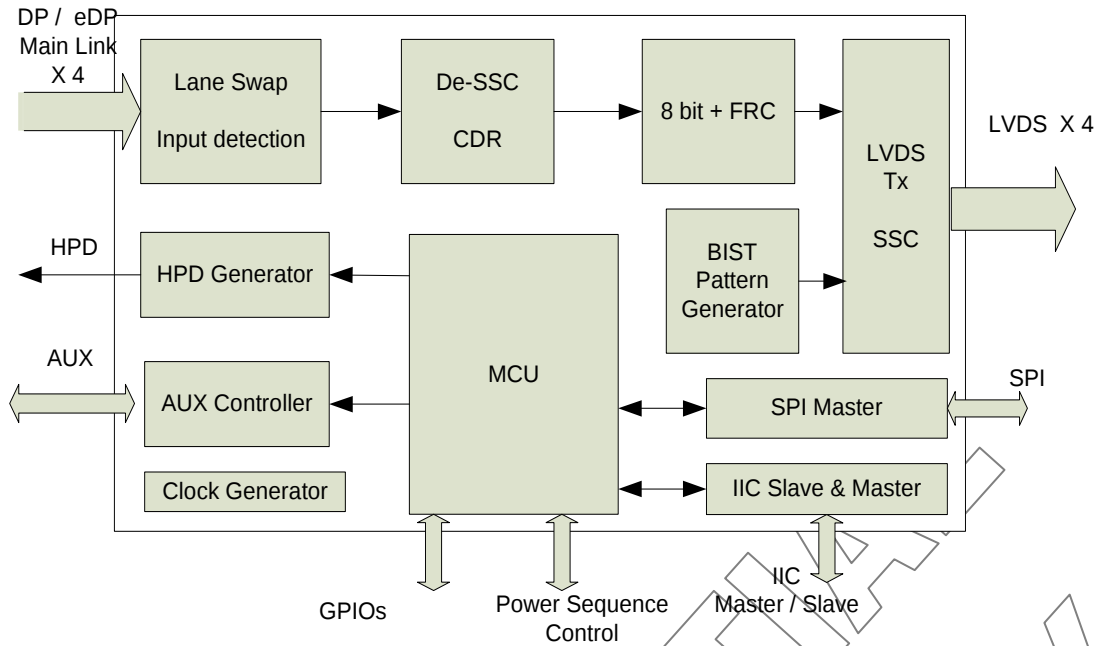


Figure 1: CH7516A Functional Block Diagram

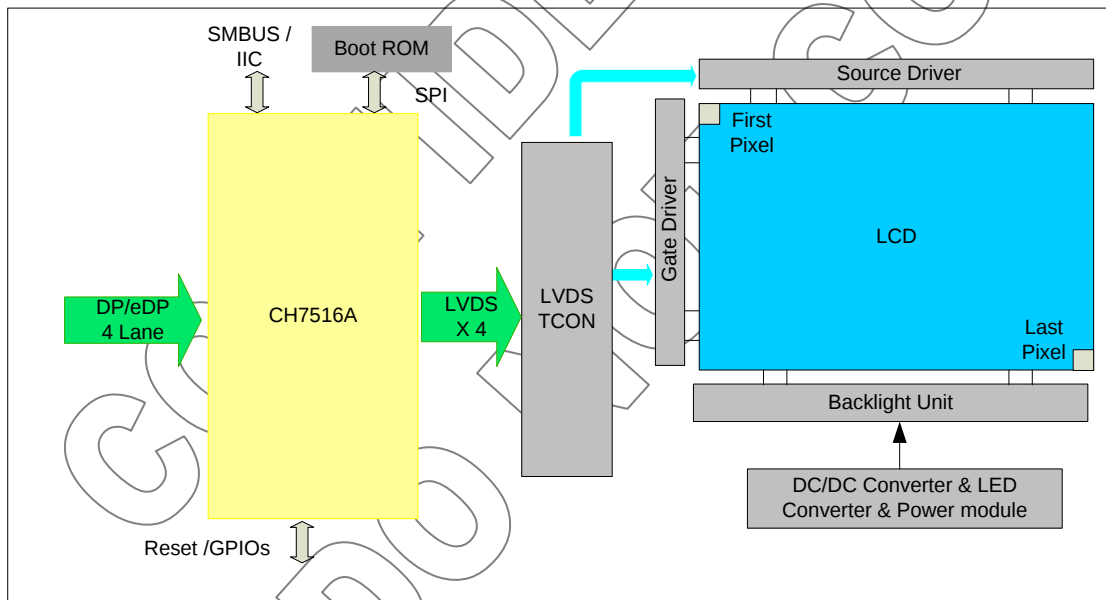


Figure 2: CH7516A Application Diagram

1.0 PIN-OUT

1.1 Package Diagram

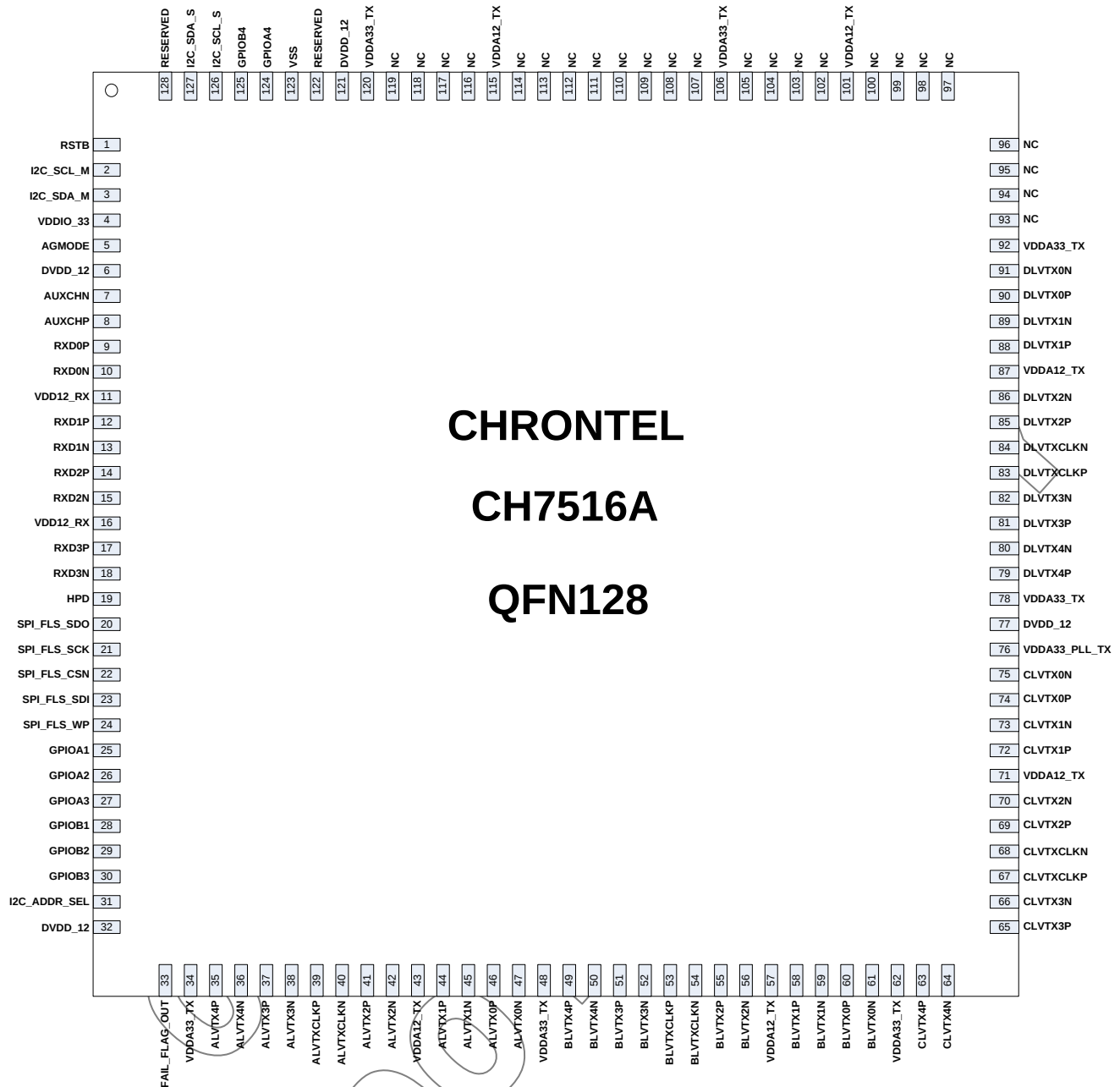


Figure 3: CH7516A 128-Pin QFN Pin Out

1.2 Pin Description

Table 1: CH7516A Pin Description

Pin #	Type	Symbol	Description
1	In	RSTB	Reset* Input (Internal pull-up) When this pin is pull low, the device is held in the power-on reset condition. When this pin is pull high, reset is controlled through the serial port register.
2	Out	I2C_SCL_M	Serial Port Clock Output for EDID/HDCP ROM This pin functions as the clock output of the serial port and operates with output from 0 to 3.3V. This pin requires an external 4k Ω - 9k Ω pull up resistor to 3.3V.
3	In/Out	I2C_SDA_M	Serial Port Data Input/Output for EDID/HDCP ROM This pin functions as the bi-directional data pin of the serial port and operates with inputs from 0 to 3.3V. Outputs are driven from 0 to 3.3V. This pin requires an external 4k Ω - 9k Ω pull up resistor to 3.3V.
5	In	AGMODE	Aging Pattern Selection AGMODE=H: and no video in: BIST pattern AGMODE=L: and no video in: black pattern (default)
7,8	In/Out	AUXCHP/N	Aux Channel Differential Input/Output These two pins are DisplayPort AUX Channel control, which supports a half-duplex, bi-directional AC-coupled differential signal.
9,10,12~15,17,18	In	RXD[3:0]P/N	DisplayPort Lane 0~3 Input One pair of differential data input. It handles clock-embedded high speed differential data input as DisplayPort standard
19	Out	HPD	Hot Plug Detect This output pin indicates whether this device is active or not. It also generates interrupt pulse as defined by DisplayPort standard. Output voltage is 3.3v.
20~24	In/Out	SPI_FLS_WP SPI_FLS_SDI SPI_FLS_CSN SPI_FLS_SCK SPI_FLS_SDO	SPI interface for Boot ROM
25~27,124	In/Out	GPIOA[4:1]	General Purpose Input/Output
28~30,125	In/Out	GPIOB[4:1]	General Purpose Input/Output
31	In	I2C_ADDR_SEL	IIC Slave Address Selection
33	Out	FAIL_FLAG_OUT	Fail Flag Output
35~42,44~47	Out	ALVTX[4:0] P/N, ALVTXCLKP/N	The First Channel LVDS Output
49~56,58~61	Out	BLVTX[4:0], BLVTXCLKP/N	The Second Channel LVDS Output
63~70,72~75	Out	CLVTX[4:0], CLVTXCLKP/N	The Third Channel LVDS Output
79~86,88~91	Out	DLVTX[4:0], DLVTXCLKP/N	The Fourth Channel LVDS Output
93~100,102~105, 107~114,116~119	Out	NC	Not Connected Pins
122,128		RESERVED	Reserved Pins
126	In	I2C_SCL_S	Serial Port Clock Input for CH7516A IIC Slave This pin functions as the clock input of the serial port and operates with inputs from 0 to 3.3V. This pin requires an external 4k Ω - 9k Ω pull up

			resistor to 3.3V.
127	In/Out	I2C_SDA_S	Serial Port Data Input / Output for CH7516A IIC Slave This pin functions as the bi-directional data pin of the serial port and operates with inputs from 0 to 3.3V. Outputs are driven from 0 to 3.3V. This pin requires an external 4k Ω - 9 k Ω pull up resistor to 3.3V.
4	Power	VDDIO_33	Digital I/O Power Supply (3.3V)
6,32,77,121	Power	DVDD_12	Digital Power Supply (1.25V)
11,16	Power	VDD12_RX	DP Rx Power Supply (1.25V)
34,48,62,78,92,120	Power	VDDA33_TX	LVDS Power Supply (3.3V)
43,57,71,87,101,115	Power	VDDA12_TX	LVDS Analog Power Supply (1.25V)
76	Power	VDDA33_PLL_TX	LVDS PLL Power Supply (3.3V)
123, E-PAD	Power	VSS	Ground

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2.0 PACKAGE DIMENSIONS

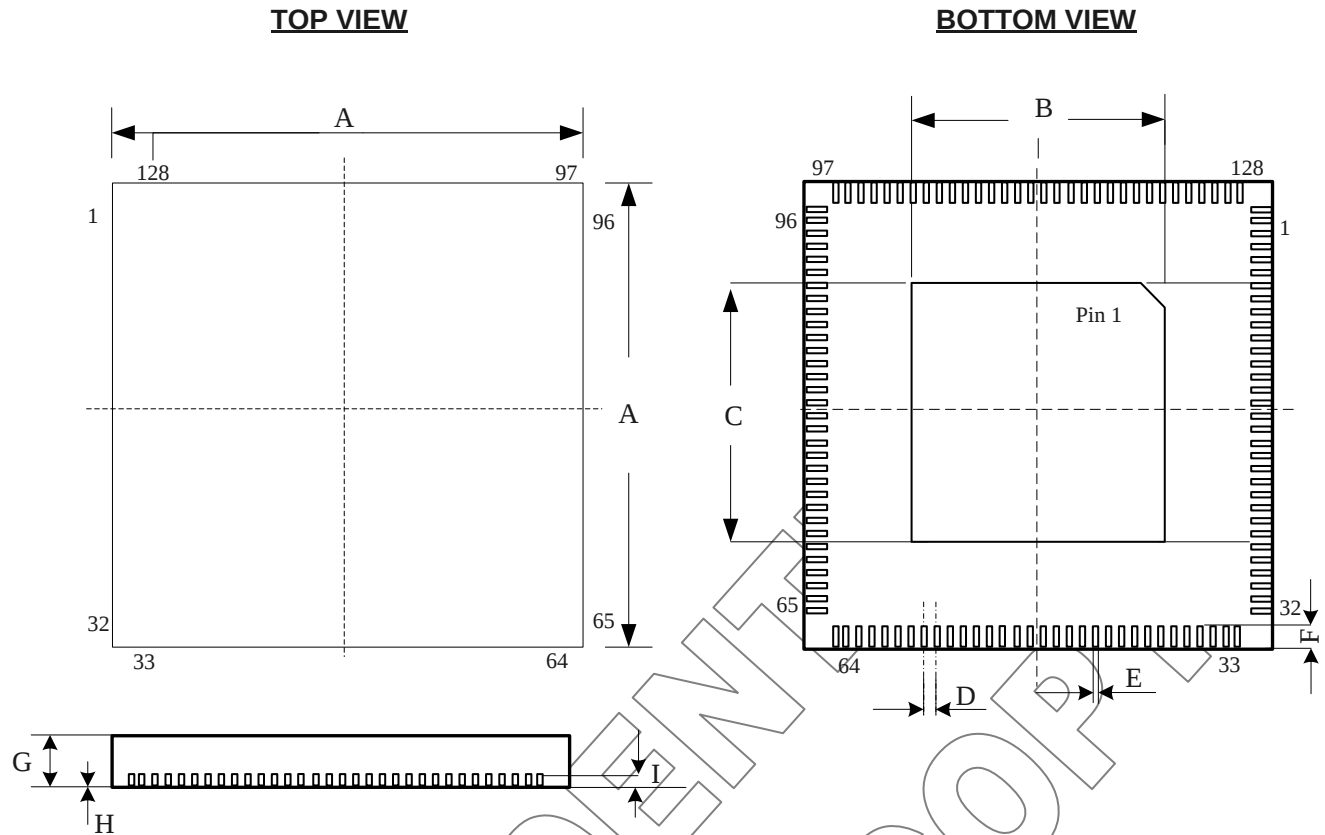


Figure 4: 128 QFN Package (12.5x12.5 mm)

Table of Dimensions

No. of Leads		SYMBOL								
128 (12.5x12.5 mm)		A	B	C	D	E	F	G	H	I
Milli- meters	MIN	12.4	6.5	6.5	0.35	0.1	0.3	0.7	0	0.15REF
	MAX	12.6	6.7	6.7	BSC	0.2	0.5	0.8	0.05	

Notes:

1. All dimensions conform to JEDEC standard MO-207.

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ORDERING INFORMATION			
Part Number	Package Type	Operating Temperature Range	Minimum Order Quantity
CH7516A-BF	128 QFN, Lead-free	Commercial: 0 to 70°C	119/Tray
CH7516A-BFI	128 QFN, Lead-free	Industrial: -40 to 85°C	119/Tray

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